DSP Implementation of a Video Bitrate Transcoder

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Abstract – Solutions are researched with which help it is possible to implement video bitrate transcoder. Digital signal processors are offered for this purpose. Measurements of implemented transcoder performance parameters are carried out for selected general purpose processors and specialized microcontroller.

Keywords – video transcoder, open loop, bitrate, quantization, DSP, application, C/C++ code.

I. INTRODUCTION

Communication networks place bandwidth constraints on video transmission. Original video content usually compressed at a high bit rate to keep video quality close to the original. The network bandwidth limits require the video data to be converted to lower bit rate by real-time video transcoding before transmission. Video transcoding algorithms use information from input compressed video streams to simplify computation and to improve video quality. In this paper, we propose a digital signal processor (DSP) implementation of a low complexity open loop MPEG-2 video transcoder, working entirely in the frequency domain [1].

II. MAIN PART

There are different platforms with different features. ASICs (Application Specific Integrated Circuit) or ASSPs (Application Specific Standard Product) are ICs (Integrated Circuit) customized for a particular use, rather than intended for general-purpose use, FPGAs (Field Programmable Gate Array) are integrated circuits designed to be configured by the customer or designer after manufacturing, DSPs (Digital Signal Processor) are specialized microprocessors with optimized architecture for fast operational needs of digital signal processing and CPUs the more and more powerful general purpose microprocessors.

Open-loop architecture for video transcoder is proposed, since open-loop transcoding operates directly on the DCT (Discrete Cosine Transform) coefficients. In open-loop transcoders, shown on Fig. 1, versus direct and close-loop transcoders, the process of video coding is reversed until the quantization step, a new quantizer value is calculated for lower bitrate, then the DCT coefficients requantized with this new quantizer value - without inverse DCT transformation, and the rest of the video coding process is executed again with the new DCT coefficient values.

To implement open-loop transcoder the DSP platform is offered, because DSPs and SIMD (Single Instruction, Multiple Data) instructions are effective for applications that are highly parallelizable and require execution of the same operation over and over again; they are less effective for applications with less uniform computational demands.

Fig. 1. Open-loop transcoder: VLD - Variable Length Decoder, Q – Quantizer, Q-1 – Dequantizer, VLC – Variable Length Coder

In the 1st and 3rd rows of Tab. 1 the average frame time and its normalized value relative to 2 GHz processors in microseconds are shown that were measured while transcoding 200 video frames from the input video stream. In 2nd and 4th rows we can see the average number of frames and its normalized values that can be transcoded in one second.

III. CONCLUSION

The experimental results show that C/C++ code running on a DSP has comparable speed clock-for-clock to older superscalar general purpose processors. However modern processors are much faster and the highest clock frequency of modern DSPs are only in the 1GHz range.

Running the same C/C++ code on DSP as on general purpose processor is the first step in DSP development, with optimized C/C++ code and using some optimized assembly code we expect achieving better DSP performance.

REFERENCES