Наноструктуры и нанотехнологии в электронике

УДК 621.383

G. Mladenov, DSc., V. Spivak, PhD., E. Koleva, PhD., A. Bogdan, S. Zelensky

Micro-and nanostructures in modern memory devices

Электронные запоминающие устройства являются важной частью современных информационных и коммуникационных систем, определяющих в значительной степени параметры и возможности системы в целом. Рассмотрены принципы работы и параметры динамических запоминающих устройств (ЗУ) с произвольным доступом к информации, выполняющие роль оперативной памяти и флеш-памяти, успешно и широко применяемые как носитель информации для ввода - вывода данных и их хранения.

Electronic storage devices are an important part of modern information and communication systems, defining the parameters and possibilities of the whole system. In this paper it is shown the operating principle and parameters of dynamic random-access storage media, working as operative memory in computer systems as well as the flash-memories, wide and successive used as input and output of data and to keep it out of information systems.

Keywords: *Nanoelectronic memory devices, Dynamic random-access memory, Flash memory.*

Introduction

Storage devices in information systems play a leading role. Nanoelectronics has accelerated the miniaturization, enhanced functions and features not only computers but also mobile (cellular) phones with cameras, music players and other electronic systems. In connection with the improvement of information systems and compete among different types of storage devices (memory), the number of their varieties is growing. However, by the type of physical effect, it is easy to divide them into two groups: electronic and magnetic storage. This paper examines the development of modern electronic memory. They perform the role:

- operational computer memory, where the volume and speed of information exchange of these components is a key parameter for the quality of the entire computer system;
- media information for the input-output data, their transportation and storage outside the information systems.

Electronic memories can be dynamic and static. The first type must be able to overwrite the stored data during storage. The main disadvantage of electronic storage (except for flash memory) - is the need of power supply in the time of recorded information storage.

1. Electronic storage devices

Consider the prospects of micro-and nanoelectronic memories, in particular, the operational dynamic and flash memory.

Integrated memory device must remain safe and as long as possible a large amount of data to allow fast input and output of information with minimal power consumption. The main functional element of integrated memory devices is a cell containing a minimum number of integrated elements.

Dynamic memory device with random access (DRAM) are composed of cells that memorize one or four bits (in a binary system of calculation). They consist of capacitors and transistors. Capacitor is charged, if the cell is stored one bit, or discharged, if the cell is stored a zero bit. Transistor connected to the capacitor is required as a controllable resistor for capacitor's charge and to keep this charge as long as possible. The capacitors in the dynamic storage aren't very large (this is due to minimization of the area and price, as well as with increasing speed). With decreasing feature size of dynamic memory designers have combined field-effect transistor with a capacitor, and thus have a record of small size and price of dynamic memory devices. At the same time, with a further scaling of the capacitor is becoming very small and must be replaced by the the second field transistor to increase the charge extracted in reading the recorded information. In the absence of power RAM is cleared, ie, the recorded information is lost.

As managed resistive element, except the inversion channel field transistors, in the recent years it is started to be applied the tunnel junctions. The most effective proposal for the creation of new electronic memory was the use of field-effect transistor with floating gate (Fig. 1).

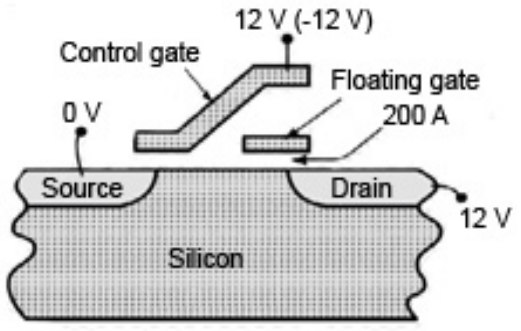

Fig. 1. The scheme of field-effect transistor with floating gate

Fig. 1 shows that the control and floating gate embedded in an insulator(not shown in the diagram). The distance from the floating gate to the silicon surface is less than 20 nm (usually around 10 nm). In this transistor, a low gate voltage is equal to one.

During the process of programming in the transistor with a floating gate it is applied a high voltage (about 12) to the control gate. High voltage creates an electric field and the tunnel effect emerges. The injection of the electrons occurs (ie, write data). Electrons tunnelling from the channel to the gate and from the channel to the floating gate can be controlled accurately (remember the Coulomb blocking). This charge, which can be stored for several years, changes the width and the conductivity of the channel that is used for reading the recorded information. It may be noted that the energy consumption during recording and reading of data is different.

During the process of erasing the control gate is fed by negative the voltage (12 V), and the electrons are tunnelling from floating gate to the source of the transistor.

On the basis of these transistors in 1984, Fujio Masuoka gave a presentation of a new memory, called *flash memory*. The first commercial integrated circuit (IC) was made in 1988. Nowadays flash memory storage capacity is up to 128 GB. This is the most well-known silicon electronic memory, which in the early-00's replaced the floppy disks.

The channel length of transistors is 30-40 nm. It should be noted that the flash memory devices have two types of architecture: "NOT-AND" or "NOT-OR" (NAND and NOR). Type "NOR" was the first; architecture "AND NOT" appeared later.

In the case of architecture type "NOR" each transistor should have an individual contact, which increases the size of the circuit. "NAND" architecture doesn't need compound to each transistor and it wins in the size, price and performance. However, these architectural solutions do not compete because each of them has their applications. The idea of transistors with floating gate, which can be called a harbinger of nanoelectronic elements in electronic memory, was further developed in the devices of the quantum dot memory, in which the floating gate is replaced by nanoparticles (quantum dots). The role of these local floating gates operates silicon or germanium crystal grains with nanosizes, located near the border gate of silicon oxide and the channel (Fig. 2).

Transistor with nanoparticles that serve as a floating gate can be made by the complementary technology. Tunnelling allows controlling the charge on each nanoparticle. In the transistors with a floating gate about 105 electrons involved in the process of tunnelling. The usage of complementary technology allows a single particle to be tunnelled by 10 electrons (for reliability). That reduces power consumption. There are implemented modules with a 128 MB and 256 MB. The disadvantage is the need of transition from thermal randomly obtained nanocrystals from an initially deposited amorphous very thin film of silicon or germanium to the structure with strictly defined parameters, produced by a given process technology.

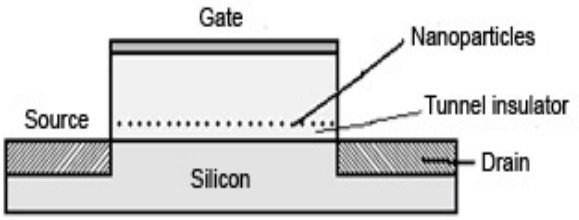

Fig. 2. The circuit in transistors with nanoparticles

The chain of sequentially placed on the facility conducting islands (quantum dots), between which tunneling is possible, is named *multitunnell junction* (MTJ). The appropriate type of memory is called the memory for multitunnell transition. These devices are still the only practical implementation of the single-electron transistors. They can be used both in binary logic and the logic of using a few (multistable) states.

Schematic diagram of the multitunnell device shown in Fig. 3. The design of the device [1, 2] made on the basis of gallium arsenide, presented in Fig. 4 δ-doped silicon layer is formed In a substrate of gallium arsenide by the method of organometallic chemical deposition (MOCVD). Then on the substrate surface to a depth of 120 nm gallium arsenide is etched. At the same time it is formed the region with quantum dots and a side gate, which can be used to manage the process of Coulomb blockade.

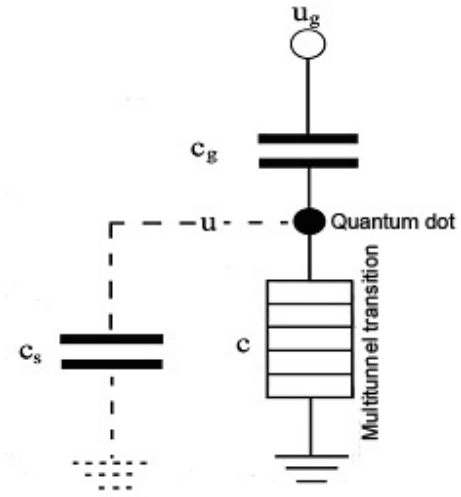

Fig. 3. Schematic diagram of single-electron memory cell

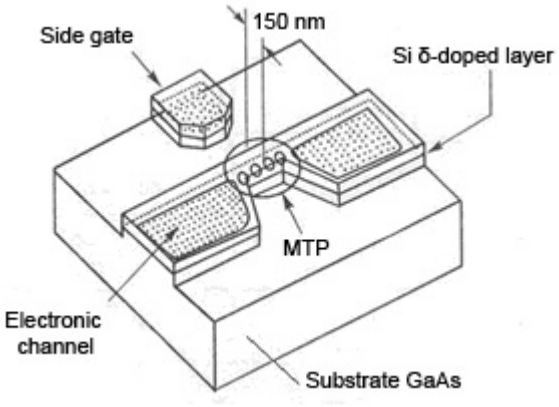

Fig. 4. Diagram of the device with multitunnel transition and side-gate

On the basis of the instrument with multitunnell transitions it is developed a memory cell, shown schematically in Fig. 3. When it is given a positive voltage impulse U_g, which magnitude is sufficient to overcome the Coulomb blockade, the capacitor C_g is charged to the appropriate voltage. With decreasing values of U_g with subsequent conversion to a zero, the capacitance C_g begins to be discharged until the discharge process does not interrupt the Coulomb blockade. At this moment, a device with multitunnell transitions will have an excess of electrons and the voltage U is less than zero. Near the voltage of Coulomb blockade $U_{k.b}$ provided $U \geq -U_{k.b}$ it is being recorded a logical zero. In case of a negative voltage pulse U_g the U value will be more than zero and will be located near the positive voltage of Coulomb blockade. In other words, $U \leq U_{k.b}$ and being recorded a logical unit.

The design of a storage cell (Fig. 4.) due to its characteristic (δ-doped S_i layer *GaAs* with capacitance *C=5aF* and gate capacitance C_g*=200aF*; parasitic capacitance C_s*=200aF*) allows you to store 1 bit of information by exploiting 40 electrons. For use at room temperature the cell size should be 5 nm.

2. Parameters of modern electronic storage devices

Table 1 lists the characteristics of today's dynamic random-access storage (dynamic random access memory-DRAM), static electronic memory with random access to recorded information (static random access memory - SRAM) and two types of flash memory with different critical dimensions, obtained in the lithographic technology of their nanostructure.

Conclusions

Electronic memory is being constantly improved under the pressure of development of magnetic storage devices and at the present stage they've helped to create a compact portable computers and communication devices. However, with decreasing the size of memory cells, it is increasing the problems of a physical nature (such as tunneling, the functioning of small groups of atomic particles as in electronic devices with micrometer or millimeter-size, heat dissipation) or technological problems (lithography structures with critical dimensions of about 5.8 nm, the defects in such nanostructures). That's why the search of new principles and new ideas occupy the attention of researchers and are widely discussed.

Table 1. Parameters of modern electronic storage devices

	DRAM	SRAM	FLASH[1]	FLASH[2]
Crit. size of the elements [nm]	90	90	90	32
Cell size [μm^2]	0,25	1-1,3	0,1	0,02
Recording Density [$Mbit/sm^2$]	256	64	512	2500
Casting Time [ns]	10	1,1	10-50	10-50
Prog. time [ms]	10^{-2}	$1{,}1.10^{-3}$	0,1-100	0,1-100
Prog. energy/bit [pkJ]	5	5	30-120	10

References

1. *Драгунов Б.П.,* Неизвестный И.Г., Гридчин В.А., Основы наноэлектроники, Москва, Логос, 2006.
2. *Lakthakia A. (ed.)* The Handbook of Nanotechnology. Nanometer structures: Theory, Modeling, and Simulation. SPIE Press, Bellingham, WA, USA, 2004
3. *Младенов Г.М.,* Спивак В.М., Колева Е.Г., Богдан А.В., Наноэлектроника: 1 книга, Введение в наноэлектронные технологии, Киев-София, Аверс, 2010
4. *Младенов Г.М.,* Спивак В.М., Колева Е.Г., Богдан А.В., Функциональные микроэлектронные компоненты с использованием квантового эффекта спинового состояния электронов и их переноса, Международная научно-техническая конференция :"Автоматизация: проблемы, идеи, решения 2010", Севастопольскии НТУ, Севастополь, 6-9 сентября 2010г.

Национальный технический университет Украины «Киевский политехнический институт»